EEStor's Composition Modified Barium Titanate (CMBT) in Multi-Layer Ceramic Capacitor (MLCC) Applications

CMBT used to create capacitors utilizing MLCC standard processes

EEStor Corporation (TSXV:ESU), developers of high energy density, solid-state capacitors, announce the results of independent third party production and testing of Multilayer Ceramic Capacitors (MLCCs), made with EEStor's proprietary Composition Modified Barium Titanate (CMBT) powder.

In a first for the MLCC industry, EEStor's CMBT powder has been used to create densified ceramic layers and Multilayer Ceramic Capacitors through standard Multilayer Ceramic Capacitor processes.

During production tests, EEStor's CMBT was used to create MLCC devices and densified layers with high relative permittivity, high insulation resistance and low dissipation. Proving that EEStor's high permittivity CMBT powder is compatible with standard MLCC manufacturing techniques.

EEStor's proprietary and patented CMBT powder was used by MRA laboratories to produce densified ceramic layers without electrodes called "K-squares" as well as size .0805 MLCCs through MRA's standard MLCC processes. These ceramic layers were made without glass binders. The raw powder was mixed with MRA standard organic binders to make a slurry for casting. Since these binders burn away during the sintering process the performance of the powder alone can be investigated. Testing to characterize these densified ceramic layers and MLCCs has been completed by Intertek, MRA and Radiant Technology. This report will detail and analyze these results.

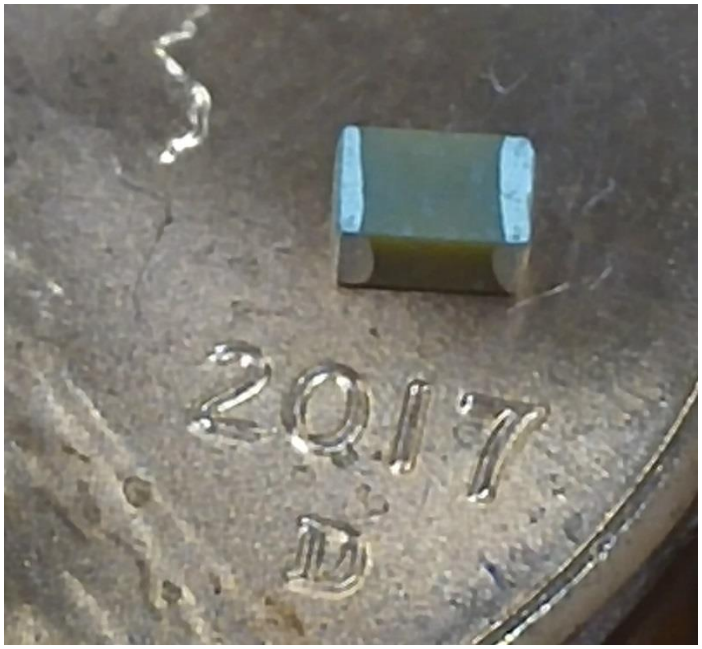

Figure 1. EEStor .0805 MLCC displayed on a Penny

K-Squares and MLCC manufacturing

MRA produces K-squares to understand the properties of the ceramic powder that will be used to make MLCCs. They do this by making a stack of densified ceramic layers stacked together without internal electrodes allowing the relative permittivity or "K" of the material to be determined along with insulation resistance and dissipation factor. K-squares are produced by following the same steps used to make an MLCC except for the printing of the internal electrodes.

First the ceramic powder is mixed with an organic binder to produce a slurry for easy handling purposes. This slurry is then cast into thin flexible green tape layers. These layers are the dielectric layers that will make up an MLCC and a K-square. If an MLCC is to be made, electrode paste is printed onto the layers at this stage. However, for a K-square no electrode is printed. The green sheets are then stacked and pressed together in a step called lamination. The organic binder from the slurry is burnt out at low temperatures, until there's no trace of it left, then the remaining ceramic powder is sintered at the final sintering temperature creating a densified ceramic sheet that is then cut into individual parts for testing. If the sheets were printed with electrode paste the paste has formed metal electrodes during the sintering between the layers and the cut parts that include these metal electrodes are MLCCs. They are then tumbled to remove rough edges and dipped in a metal solder paste to provide connectivity to the internal electrodes. If on the other hand the layers were not printed with electrodes the parts after slicing are called K-squares and electrodes are sputtered on the surface for testing of the dielectric's properties.

Third Party Testing and Validation

EEStor's Composition Modified Barium Titanate (CMBT) is the foundation for creating very high permittivity dielectric materials. These dielectrics have been tested extensively over a three-month period by three independent parties - Intertek, Radiant Technologies and MRA Laboratories. To learn more about test results, See:

- MRA MLCC Test Results
- Radiant Phase 9 Test Results
- Intertek Phase 9 Test Results
- MRA K Square Test Results
- MRA Post-Process Test Results

K-Square Results

Intertek, MRA Laboratories and Radiant Technologies all tested two different versions of the K-squares produced by MRA. One version was as manufactured and delivered by MRA the other versions were all post processed by sintering for an additional 2 hours at 1320 °C in air.

Sample ID	Test voltage	Post Processed	Estimated Permittivity	Testing Org.
# 2000	75 VDC	No	12359	Intertek
# 2001	75 VDC	No	10494	Intertek
# 1056	75 VDC	Yes	37050	Intertek
# 1062	75 VDC	Yes	30672	Intertek
# 1095 (L3)	300VDC	N o	12308	Radiant
# 1053 (L2)	300VDC	Yes	28171	Radiant
# 1082	1 VAC	Yes	22034	MRA
# L-3H	1 V AC	No	8218	MRA

Figure 2. Sample List as Tested

This drastic change in permittivity with additional sintering time, indicates higher permittivity can be achieved in initial production if higher sintering temperature and or longer sintering time are used.

The following graphic shows the Polarization to Electric Field hysteresis plot (PE loop) measured by Radiant on as delivered K-square #1095 and on post-processed K-square #1053. PE loop plots illustrate many aspects of the capacitor's performance. The bottom trace of each loop represents the charge portion of the charge discharge cycle, the top line represents discharge as the capacitor voltage returns

to 0. The slope of the PE loop trace is the capacitance at that point on the curve, the area between the charge and discharge curve is the energy lost in one charge and discharge cycle. It can be seen from the plots that both capacitors have low residual polarization and very low losses. It can also be seen from the plot of the "as-manufactured" K square (green PE loop) that the peak of the loop does not reach the same level of polarization as the post processed PE loop in red. This is in spite of the "as-manufactured" capacitor experiencing a higher electric field. This is because the slope of the green line is significantly less than the slope of the red line at low voltages demonstrating that the post processed sample has much higher capacitance at low voltages resulting in the larger permittivity at low voltages which in turn leads to more polarization per unit of electric field. The permittivity for #1053 is 28171 at .5v/micron while #1095 has a K of 8232 at . 5v/micron. Yet, at high electrical field, the slope of the two lines are nearly the same: Sample #1053 has a K of 2745 and #1095 a K of 2156, which is nearly the same permittivity near breakdown. The energy stored is the area to the upper left of the curve on this chart defined by the y axis at 0 volts, the discharge curve of the loop and a line from the peak of the loop to the Y axis parallel with the X axis as shown. The area outlined by the pink line represents the energy stored in capacitor (L2)#1053(0.3 J/cc) at that voltage, whereas the area outlined by the lime green line represents the energy stored in capacitor (L3) #1095 (0.409 J/cc) at that voltage.

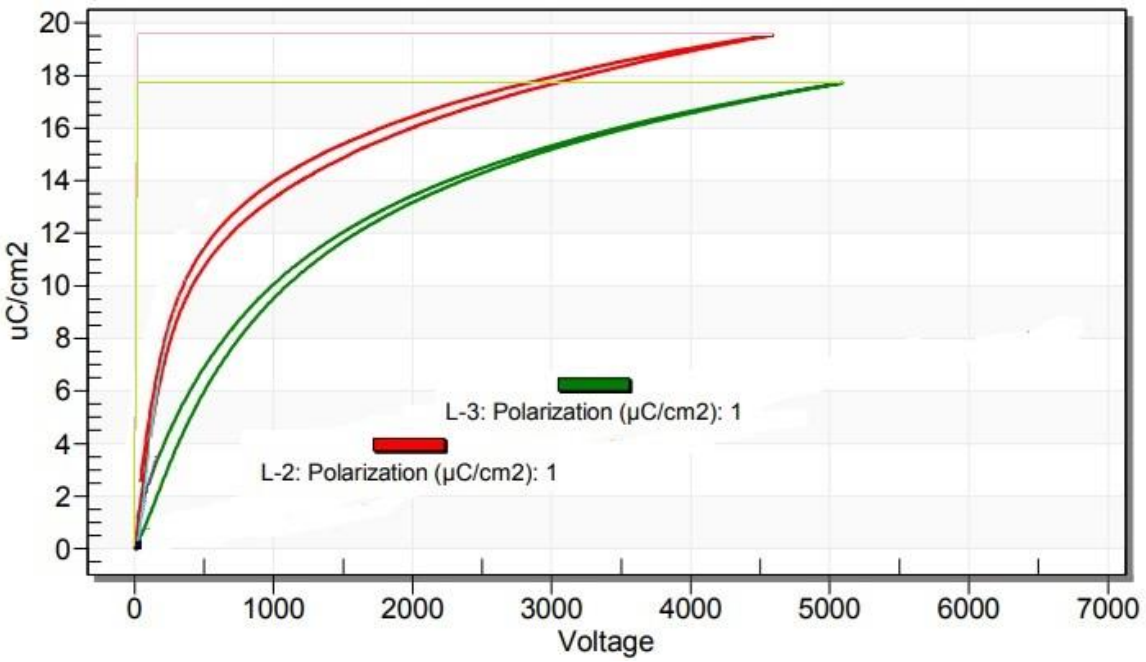

Figure 3. Polarization vs Electric Field Plots for (L2) #1053 and (L3) #1095

It is interesting to note that the higher capacitance sample with the larger polarization does not store the most energy but instead it is the lower capacitance sample with 500 volts more field that holds more energy. This difference in energy recovered and stored is related more to the shape of the polarization curve than it is to the magnitude of the voltage. As can be seen when both parts were tested by Radiant at 4600V, the lower K sample #1095 has a higher energy recovered and stored because the integrated area is larger due to the shape of the polarization curve. Depending on the requirement of the application, the MLCC process could be tuned for either high relative permittivity (k) or high energy density.

			Energy in Joules/cc		
	DC volts	Volts/μ	Stored	Recovered	η
#1053	4600	7.9	0.3766	0.3489	92.66%
#1095	4600	8.2	0.3458	0.3095	89.50%

Figure 4. Energy stored and recovered from # 1053 and #1095 at 4600V

Thus, the high K part will be the best suited for an application where the primary consideration is capacitance and the lower K sample will be a better choice for energy storage applications.

MLCC Results

MLCCs were produced by MRA laboratories from EEStor's CMBT powder. The MLCCs were sintered at 1300°C in air. The MLCCs were produced in the 0805case size (2mm x 1.25mm x .9mm), in a parallel design and contain 22.5 active layers. Dielectric layers are a thickness of 19.7 μ, and internal electrode layers are approximately 2.5 μ thick each with an area of 1156 μ x 560 μ or 647360 μ^2 . The MLCCs showed a maximum capacitance of 94 nF giving a relative permittivity (K) of 14262 at 1volt rms 20hz. Insulation resistance of the MLCCS was found to be 4.5 tera-ohms at room temperature insulation resistance at 125 °C was found to be 1.8 tera-ohms. The DC breakdown voltage was found to be 45.9 V/μ or 905Volts.

MRA performed Highly Accelerated Life Testing on the MLCCs . In this test the MLCCs were exposed to 200VDC and 180 °C for 100 hours. MRA found that 20 out of 20 passed HALT testing with no failures and an Insulation resistance at 1 terra ohm after 100 hours. HALT testing is performed to get information on the reliability of a product. With all 20 of the samples passing the HALT test with no significant degradation in resistance suggesting the parts have high predicted reliability/lifetime.

Test #6: Highly Accelerated Life Test
(@ 200Vdc, 180°C, 100h)

Time, h	LT-4775 MLCC (average of 20 chips), IR, Ω	Amount of failures
2	$1.6*10^{12}$	0/20
12	$1.2*10^{12}$	0/20
24	$1.2*10^{12}$	0/20
36	$1.1*10^{12}$	0/20
48	$1.1*10^{12}$	0/20
60	$1.1*10^{12}$	0/20
72	$1.0*10^{12}$	0/20
84	$1.0*10^{12}$	0/20
96	$1.0*10^{12}$	0/20
100	$1.0*10^{12}$	0/20
Used equipment: Custom made HT-HALT system. Measured uncertainty: IR ±0.25%. Room temperature: 24.7°C. Relative humidity: 52.0%.		

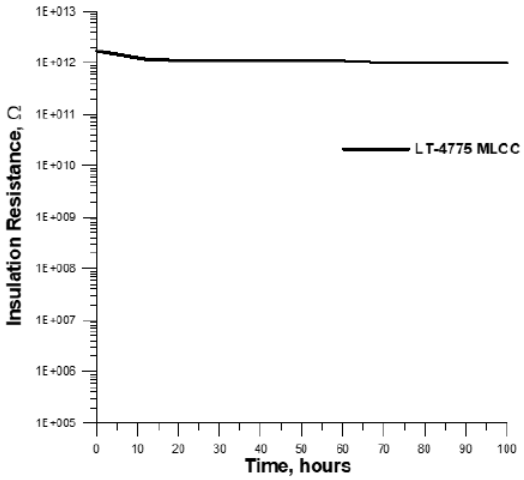

Figure 5. Highly Accelerated Life Test Results

Thermal testing of completed MLCCs show these parts' capacitance drop by 81% at -45°C and drop by 76% at 125°C and 53% by 85°C meeting the Y5V and Y7V Electrical Industry Alliance (EIA) RS-198 standard for capacitor thermal performance at 0 Volts and the X7V Standard in the 200V DC bias tests.

Test #3: Temperature Coefficient of Capacitance
(@ 1 kHz, 1Vrms, -55°C – 200°C temperature range, 0V dc-bias)

Temp., °C	LT-4775 MLCC (average of 3 chips)	
	Cap, %	DF, %
-55	-84.241	16.663
-45	-81.058	19.514
-35	-76.887	23.449
-25	-71.448	28.257
-15	-63.091	32.985
-5	-49.649	36.521
5	-26.885	35.974
15	-2.207	27.795
25	0.000	16.395
35	-9.884	8.596
45	-22.850	5.473
55	-34.704	4.080
65	-44.669	3.301
75	-52.825	2.679
100	-69.250	1.469
125	-80.153	0.695
150	-86.494	0.364
175	-90.186	0.200
200	-92.449	0.107
Used equipment: HP 4278A Capacitance meter and Delta 9023 environmental chamber. Measured uncertainty: C, DF ±0.25%. Room temperature: 24.7°C. Relative humidity: 52.0%.		

Figure 6. Temperature Coefficient of Capacitance at 0 V DC bias

Test #4: Temperature Coefficient of Capacitance at dc-bias
(@ 1 kHz, 1Vrms, -55°C – 200°C temperature range, 200V dc-bias)

Temp., °C	LT-4775 MLCC (average of 3 chips)			
	0V dc-bias		200V dc-bias	
	Cap, %	DF, %	Cap, %	DF, %
-55	-81.309	14.736	-97.595	1.277
-45	-80.544	15.161	-97.488	0.702
-35	-76.615	16.637	-97.362	0.472
-25	-71.302	18.213	-97.225	0.380
-15	-63.321	19.879	-97.067	0.303
-5	-52.242	20.601	-96.882	0.095
5	-33.394	19.860	-96.681	1.901
15	-10.324	15.751	-96.494	1.552
25	0.000	10.063	-96.360	0.647
35	-1.898	5.797	-96.164	0.146
45	-12.826	3.800	-95.982	0.003
55	-24.396	3.021	-95.786	-0.010
65	-35.278	2.474	-95.585	-0.014
75	-44.540	1.980	-95.390	-0.020
85	-53.076	1.623	-95.184	-0.024
95	-60.654	1.221	-94.982	-0.027
105	-66.956	0.949	-94.792	-0.028
115	-72.208	0.645	-94.618	-0.027
125	-76.454	0.474	-94.468	-0.026
135	-79.880	0.351	-94.348	-0.026
145	-82.628	0.257	-94.260	-0.029
155	-84.844	0.183	-94.208	-0.027
165	-86.631	0.127	-94.192	-0.029
175	-88.103	0.082	-94.211	-0.031
185	-89.317	0.046	-94.263	-0.031
195	-90.336	0.021	-94.346	-0.032
200	-90.802	0.008	-94.399	-0.035
Used equipment: HP 4278A Capacitance meter and Delta 9023 environmental chamber. Measured uncertainty: C, DF ±0.25%. Room temperature: 24.7°C. Relative humidity: 52.0%.				

Figure 7. Temperature Coefficient of Capacitance at 200 V DC bias

EEStor CMBT powder was successfully made into MLCCs and densified layers through normal MLCC process. The MLCCs were tested by MRA and found to be of good quality and high performance. These MLCCs were made with CMBT and contain no glass binders as sintering aids. The MLCCs were made with precious metal electrodes due to the relatively high 1300°C sintering temperature. Spark Plasma Sintering trials have shown that glass can lower the sintering temperature further to accommodate base metal electrodes while also improving the saturation and thermal characteristics of the dielectric. EEStor's next MLCC manufacturing test will be to make hybrid dielectric MLCCs containing CMBT and Glass.

About EEStor Corporation

EEStor is a developer of high energy density solid-state capacitor technology utilizing the Company's patented Composition Modified Barium Titanate (CMBT) material. The Company is focused on licensing opportunities for its technology across a broad spectrum of industries and applications.

The Company's success depends on the commercialization of its technology. There is no assurance that EEStor will be successful in the licensing of the technology. Readers are directed to the "Risk Factors" disclosed in the Company's public filings.

For additional information please contact:

Ian Clifford
Chief Executive Officer
EEStor Corporation
Tel. 416-535-8395 ext. 3
ian.clifford@eestorcorp.com

Nick Jones
Vice President - Technology
Sparkpr
Tel. 44-7832115362
Nick.jones@sparkpr.com

Neither TSX Venture Exchange nor its Regulation Services Provider (as that term is defined in the policies of the TSX Venture Exchange) accepts responsibility for the adequacy or accuracy of this release.